REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application, and for allowing Claims 71-74.

The Examiner rejected Claims 39-55 as being indefinite. In particular, the Examiner has taken the position that the claim recitation of "incrementing, decrementing or two's complementing a first string of N bits" is not supported by the current claims for providing the detailed steps/physical structure necessary to perform theses steps.

Independent Claim 39 recites generating an auxiliary string of *N* bits as a function of the first string. The auxiliary string has a first least significant bit that is independent from the first string and any other bit of the auxiliary string. Starting from a second least significant bit up to a most significant bit of the auxiliary string, a logic combination is performed with a corresponding bit of the first string or a negated replica thereof, starting from a least significant bit up to a second most significant bit of the first string, and of the bits of the first string or the negated replica thereof less significant than the corresponding bit. An output string is generated as a logic combination of the auxiliary string and of the first string.

The Examiner has taken the position that independent Claims 39 and 55 correspond to FIGS. 6A and 6B, which show only two's complement circuits; and consequently, the independent

claims do not perform the incrementing and decrementing functions as claimed.

Referring to FIGS. 6A and 6B, the auxiliary string is represented by M, $\overline{M}$, and the first string is represented by X. Independent Claim 39 recites that a logic combination is performed when generating the auxiliary string. Based upon the results of the logic combination (the logic combination could be an OR mask or an AND mask as respectively shown in FIGS. 6A and 6B), the output string (represented by Y) is generated as a logic combination of the auxiliary string and of the first string. The logic combination is the same in FIGS. 6A and 6B for generating the output string Y. Dependent Claims 43 and 44 are respectively directed to the logic combination in the auxiliary string, i.e., the OR mask and the AND mask.

One embodiment for the decrementing circuit is shown in FIG. 9B, for example. The difference is the inverter in the auxiliary string path. The logic combination for the decrementing in FIG. 9B is the same as the logic combination performed in FIGS. 6A and 6B.

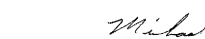
A similar comparison can be made for the incrementing. One embodiment for the incrementing circuit is shown in FIG. 10C, for example. The difference is the two inverters in the auxiliary string path. The logic combination for the incrementing in FIG. 10C is the same as the logic combination performed in FIGS. 6A and 6B.

The Applicant submits that the independent claims broadly recite generating the auxiliary string, and generating

the output string as a logic combination of the auxiliary string and of the first string. Based upon how the auxiliary string is generated, then generation of the auxiliary string will result in either incrementing, decrementing or two's complementing of the N bit string. Accordingly, the Applicant submits that the claims are definite.

In view of the remarks provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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